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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,663	08/11/2003	Wataru Itoh	60188-632	3512

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,663	ITOH ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/22/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-13 are present in this Response to applicants instant Response.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (2/13/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided after the initial application was examined and will be given consideration at this time.

Response to Arguments

Applicant's arguments filed 3/13/06 have been fully considered by the Examiner. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ellis (US 6324485).

1. As per claim 1, Ellis teaches an assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, the assembly comprising:

A peripheral circuit (components - column 3 line 64, devices – column 6 lines 3-4) coupled to the target LSI (DUT – column 1 line 33) and allowing the target LSI to operate in the same manner as in actual operation (column 3 lines 60-64, column 4 – FIG. 3B, column 6 lines 13-17, and column 7 lines 10-11);

A socket into which the target LSI is inserted (sockets – column 5 lines 54-56); and

A printed circuit board (load board - column 1 line 35, interface board - 206 figure 2 column 5 line 29) on which the peripheral circuit and the socket are mounted (column 1 lines 33-34, column 5 lines 29-30, column 5 lines 54-56, and column 5-6 lines 67-5).

2. As per claim 2, Ellis teaches the above assembly for an LSI test including:

A first board including the peripheral circuit and the printed circuit board (column 5-6 lines 67-5); and

A second board coupled to the first board (column 5-6 lines 67-5) and including wiring for coupling the first board and the LSI tester to each other (column 6 line 7 and lines 54-56).

3. As per claim 3: Ellis teaches the above assembly for an LSI test wherein the test signal is supplied to the peripheral circuit and then output from the peripheral circuit to the target LSI (column 1 lines 35-36, column 5 lines 29-31, and figures 1A and 2).

4. As per claim 4: Ellis teaches the above assembly for an LSI test wherein the test result signal is supplied to the peripheral circuit and then output from the peripheral circuit to the LSI tester (column 1 lines 35-36, column 5 lines 29-31, and figures 1A and 2).

5. As per claim 5: Ellis teaches the above assembly for an LSI test wherein a memory is provided as the peripheral circuit or in the target LSI (column 5-6 lines 67-5), and the LSI tester is configured to be capable of accessing the memory asynchronously to a clock supplied to the target LSI (column 3 lines 62-67).

6. As per claim 6: Ellis teaches the above assembly for an LSI test wherein the test signal is stored in the memory, and then read out from the memory to be processed by the target LSI (column 5 lines 31-32 and lines 45-48).

7. As per claim 7: Ellis teaches the above assembly for an LSI test wherein the test result signal is stored in the memory, and then read out from the memory to the LSI tester (column 5 lines 31-32 and lines 45-48).

8. As per claim 8: Ellis teaches an assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, the assembly comprising:

A test result receiving circuit for performing given processing on data obtained as the test result signal so as to reduce the amount of data, and for outputting a result of the processing to the LSI tester (ATE – column 1 lines 36-41 or column 6 lines 1-5, column 5 lines 29-31, and column 1 lines 35-36);

A socket into which the target LSI is inserted (sockets – column 5 lines 54-56); and

A printed circuit board (load board - column 1 line 35, interface board - 206 figure 2 column 5 line 29) on which the test result receiver circuit and the socket are mounted (column 1 lines 33-36, column 5 lines 29-30, column 5 lines 54-56, and column 5-6 lines 67-5).

9. As per claim 9: Ellis teaches the above assembly for an LSI test wherein an enable control circuit for selecting necessary data from the data obtained as the test result signal and for outputting the selected data is provided in the test result receiving circuit of in the target LSI (column 6 lines 1-5).

10. As per claim 10: Ellis teaches the above assembly for an LSI test wherein the test result receiving circuit includes a compression circuit for compressing input data and outputting the compressed data (column 6 lines 1-5).

11. As per claim 11: Ellis teaches the above assembly for an LSI test wherein the test result receiving circuit includes a determination circuit for determining whether or not the input data coincides with data to be input when the target LSI operates normally, and outputting a result of the determination (column 1 lines 38-41 or column 6 lines 1-5).

12. As per claim 12, Ellis teaches an LSI test system, comprising:

An LSI tester for supplying a test signal to a target LSI to be tested (column 1 lines 36-37); and

An assembly for an LSI test which outputs, to the LSI tester, a result signal generated by processing of the target LSI performed in accordance with the test signal, wherein the assembly comprises:

A peripheral circuit (components - column 3 line 64, devices – column 6 lines 3-4) coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation (column 3 lines 60-64, column 4 – FIG. 3B, column 6 lines 13-17, and column 7 lines 10-11);

A socket into which the target LSI is inserted (sockets – column 5 lines 54-56); and

A printed circuit board (load board - column 1 line 35, interface board - 206 figure 2 column 5 line 29) on which the peripheral circuit and the socket are mounted (column 1 lines 33-36, column 5 lines 29-30, column 5 lines 54-56, and column 5-6 lines 67-5).

13. As per claim 13: Ellis teaches an LSI test method, comprising the steps of:

Operating a non-defective LSI, which is configured as a target LSI to be tested and has been confirmed to operate normally, in a circuit equivalent to a circuit actually used (column 6 lines 13-17 with column 9 lines 33-34), and generating and storing a test signal and a reference test result signal, based on a signal supplied to the non-defective LSI and a signal output from the non-

defective LSI, respectively (column 1 lines 36-38, 30-33 with column 5 lines 25-26, 32-38); and

Supplying the test signal to the target LSI to compare a test result signal generated by the target LSI in accordance with the test signal, with the reference test result signal, thereby determining whether or not the target LSI is defective (column 1 lines 36-41 and column 5 lines 32-38).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The Examiner notes that the IDS submitted on 2/23/06 contains reference to the prior art used in this rejection in addition to other related art. However all this referenced

prior art was not included in the IDS submitted. Therefore all the referenced prior art has been cited on the 892. Examiner additionally notes that some of the referenced prior art was improperly numbered within the IDS contents and has been properly numbered within the 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER